

EGR 234 – Digital Logic Design
Lab 6:
Hex-to-Seven Segment Decoder Design
Using VHDL

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Exercise 1

Truth Table for the hex-to-seven segment decoder.

x(3)	x(2)	x(1)	x(0)	s(6)	s(5)	s(4)	s(3)	s(2)	s(1)	s(0)
0	0	0	0	1	0	0	0	0	0	0
0	0	0	1	1	1	1	1	0	0	1
0	0	1	0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	0	0	0	0
0	1	0	0	0	0	1	1	0	0	1
0	1	0	1	0	0	1	0	0	1	0
0	1	1	0	0	0	0	0	0	1	0
0	1	1	1	1	1	1	1	0	0	0
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	1	1
1	1	0	0	1	0	0	0	1	1	0
1	1	0	1	0	1	0	0	0	0	1
1	1	1	0	0	0	0	0	1	1	0
1	1	1	1	0	0	0	1	1	1	0

Exercise 2

VHDL Code for hex-to-seven segment decoder

```
-----  
-- hex-to-seven-segment decoder  
-- segment encoding  
-- 0  
-- ---  
-- 5 | | 1  
-- --- <- 6  
-- 4 | | 2  
-- ---  
-- 3  
-----  
library ieee;  
use ieee.std_logic_1164.all;  
  
entity hex7seg is  
    port (hex : in std_logic_vector(3 downto 0);  
          seg : out std_logic_vector(6 downto 0));  
end hex7seg;  
  
architecture hex7seg_arch of hex7seg is  
begin  
    with hex select
```

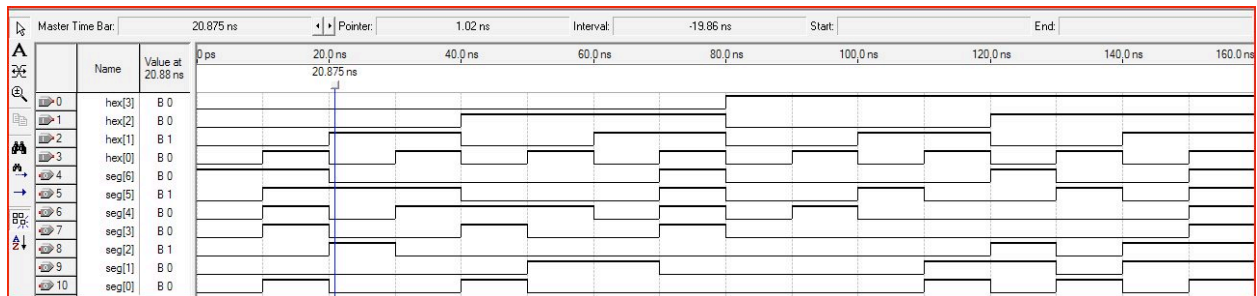
```

seg <= "100000" when "0000",
      "1111001" when "0001",
      "0100100" when "0010",
      "0110000" when "0011",
      "0011001" when "0100",
      "0010010" when "0101",
      "0000010" when "0110",
      "1111000" when "0111",
      "0000000" when "1000",
      "0010000" when "1001",
      "0100000" when "1010",
      "0000011" when "1011",
      "1000110" when "1100",
      "0100001" when "1101",
      "0000110" when "1110",
      "1111111" when others;

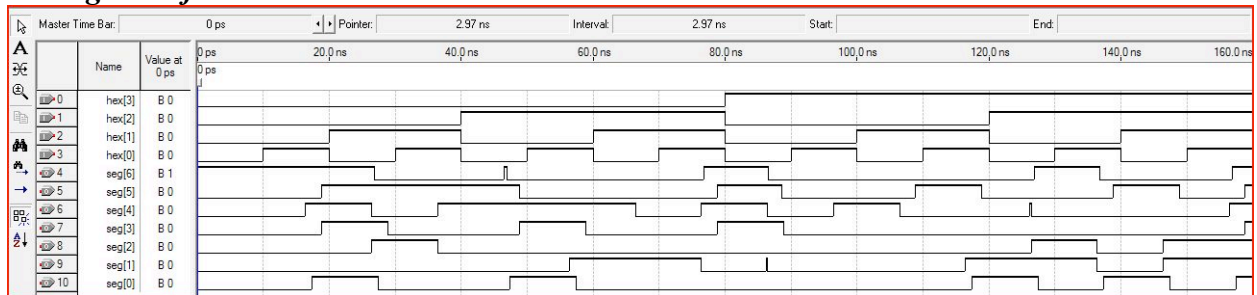
```

end hex7seg_arch;

Functional Waveform



Timing Waveform



The Functional Waveform matches up with the original truth table, which is capable of interpreting these two waveforms. The outputs also correspond to the Seven Segment Decoder LED's on the DE2 board. This confirms the program and waveforms are correct.