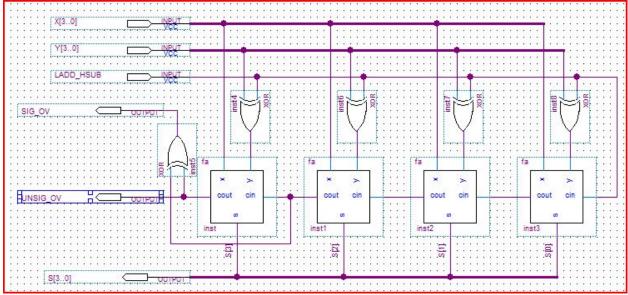
EGR 234 – Digital Logic Design Lab 9: Arithmetic and Logic Unit Design

Lab Report by: Christopher Parisi Lab Partner: No Partner November 5, 2010

Exercise 1

Schematic for the 4-bit Adder/Subtractor



Functional Waveform for the 4-bit Adder/Subtractor

1		0 ps	10.0 ns		20.0 ns		30.0 ns	41	0.0 ns	50.0 r	IS	60.0 ns	70.0	ns 80.0 r
	Name	0 ps												
@>0	LADD_HSUB													
	Ξ×		1 X	3	X	5	X	7	X	9 X	В	X	D X	F
⊡ ≥2	— X[3]		-							8				
■>3	— X[2]	-								2				
■ 4	— X[1]													
5		—		-						· ·			~ ~	5
D 5	E Y	—	<u> </u>	2		4		6	<u> </u>	<u>8 X</u>	A		<u>c X</u>	E
m 8	— Y[3] — Y[2]	1							4					
9	-Y[1]				-		_					-	F	
■ 10	-Y[0]													
a 11	🖃 S		1 X	5	X	9	Х	D	X			1		
12	— S[3]		_											
13	— S[2]								0					
14	— S[1]	-			_				_					
	S[0]				_									
• 16 - 17	SIG_OV	-												
17	UNSIG_OV				1		12							

The waveform confirms that the Adder/Subtractor circuit is functional and can be used as a module in the ALU circuit.

Exercise 2

Schematic for subcircuit 1_minmax

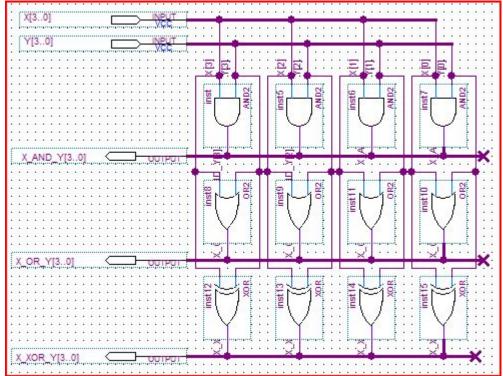
X13.01	
International Contraction of the	• mux2_4bit
Y[30]	
in propriet and a second se	×[30] 🗟
· · · · · · · · · · · · · · · · · · ·	
	f[3.0]
·····X[30] G	y[30]
······································	. inst4
Y[30] L	· potential and advantation to the standard of the second s
inst	mux2 4bit
•••••••••••••••••••••••••••••••••••••••	
	x[3.0] 0
	f[30]
· · · · · · · · · · · · · · · · · · ·	y[3.0]
	inst5
	Immenenenenenenenen

Functional Waveform for subcircuit 1_minmax

	182	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	50.0 ns	60.0 ns
	Name	0 ps						
0	ΞX	1000	χ <u>0111</u>	X O	001 X	1101 X	0010 X	0000
ii⊳ 1	—×[3]			-				
₽ 2	—×[2]							
₽ 3	—×[1]							
■ 4	-×[0]	0101	0011			1110	0010 V	0000
	E Y	0101	X 0011	X0	010 X	1110 X	0010 X	0000
	— Y[3] — Y[2]	2 						
₽7 ₽8	-Y[1]							
<u>∎</u> >9	-Y[0]							
10	MIN	0101	χ <u>0011</u>	X 0	001 X	1101 X	0010 X	0000
11	- MIN[3]							
·@ 12	— MIN[2]		8					
13	— MIN[1]							
1415		1000	X 0111		010 X	1110 X	0010 X	0000
15		1000						, 0000
10	- MAX[2]		1					
18	-MAX[1]			6				
·@ 19	MAX[0]							

The waveform confirms that the minmax circuit is functional and can be used as a module in the ALU circuit.

Schematic for subcircuit 2_logic

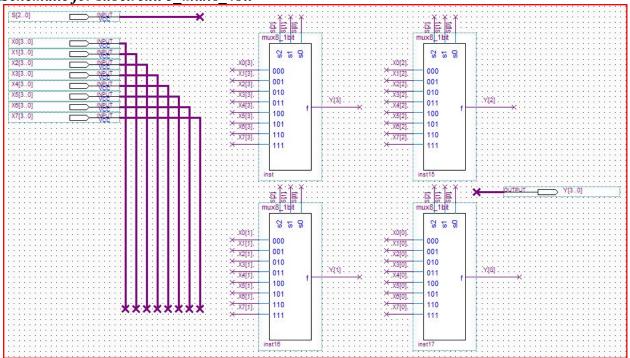


Functional Waveform for subcircuit 2_logic

	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	50.0 ns	60.0 r
Name	0 ps						
≥0 🖬 X	010	1 <u>X</u> 001	1 <u>X</u> 1010	х <u>х</u>	0110 X	1101 X	0101
▶1 —X[3]	1					1	
≥2 — X[2]							
▶3 —X[1]	-						
▶4 ×[0]							
≥5 ⊡ Y	001	1 X 001	0 X 000) <u>X</u>	1100 X	0111 X	0101
▶6 - Y[3] ▶7 - Y[2]	-						
7 − Y[2] 8 − Y[1]							
>9 L ¹ (1)							
10 E X_AND_Y	000	1 X 001	0 X 000	x x	0100 X	0101	
€ 15 E X_OR_Y	011	1 X 001	1 1010) X	1110 X	1111 X	0101
20 E X_XOR_Y	0110	000 X 000	1 X		1010	X	0000

The waveform confirms that the logic circuit is functional and can be used as a module in the ALU circuit.

Schematic for subcircuit 3_mux8_4bit



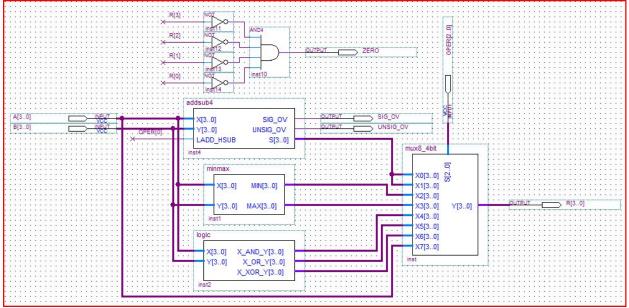
Functional Waveform for subcircuit 3_mux8_4bit

	2000	0 ps	10.0 ns	20.0 ns	30.0 ns	40.0 ns	5	i0.0 ns		
	Name	0 ps								
0	🖃 S	000	χ 00	1 χ 0	10 X	011 X	100	χ́ 101		
≥1	— S[2]	-								
2	S[1]				8					
€≪	S[0]				3					
₩4	E X0	0101	ι χ			0000				
₽9	∃ <u></u>	0000) <u> </u>	π χ		0000				
P 14	⊞ X2	k	0000	χ 01	01 X		0000			
1 9	Ξ X3		000	00	X	0101 X	X 0000			
24	⊞ X4			0000		X	0101	X 0000		
29	Ⅲ ×5			00	00			X 0101		
₩34	⊞ X6	k		1	0000					
39	Ⅲ X7	k			0000					
44	ΞY				0101					

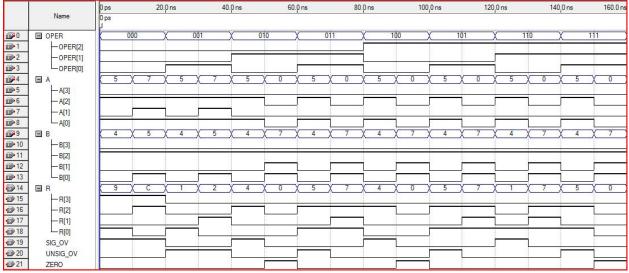
The waveform confirms that the 4bit 8-to-1 MUX is functional and can be used as a module in the ALU circuit.

Exercise 3

Schematic for the ALU



Functional Waveform for the ALU



The waveform shows that the ALU is functional and is ready to be uploaded to the DE2 board.

Schematic for the ALU to hex7seg display

PIN_U4						AL	11		······································									
PIN_U3	1					AL	10											11
L	1						Salar Carl					PIN	AB21					
	OPER[2	20]	\square	NEW .	-		OPER[20]	UNSIG_OV	OUT	PUT	UNSIG_OV	· · · ·						
N_C13	A[30]			NO T		• •				PUT	SIG_OV		AE22					• •
N AC13	M[50]			VCC	-		A[30]	SIG_0\			2 alo_0v	PIN	L_AF23					• •
	B[30]			Neut Neut Neut	10 1 1 1 1 1 1					PUT	-> ZERO							1
N_AD13			<u> </u>				B[30]	ZER	i i inge			PIN	AE23					
AF14	1/							R[30		hex7seg								
	47							inform	1.1									
	1					• •			1.			OUT	0UT	> R[6	01			• •
N_AE14						• •				hex[30]	seg[60]			rdo				• •
P25						in:	sto			10000	R 33228 19					1	N_V	11
											,							
N26																· · · F	PIN_V	/1
N25											,						PIN_A	1F
	4									inst7								
										11217						· · ·	PIN_A	4D
																	PIN_A	10
																F	N_A	٩B
																	N_A	
																		74

The circuit was compiled and uploaded to the DE2 board and the correct results were shown on the HEX display and LEDs. Each module performs each task correctly and the ALU is functional.