EGR 234 – Digital Logic Design

Lab 9:

Arithmetic and Logic Unit Design

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Lab Partner: No Partner

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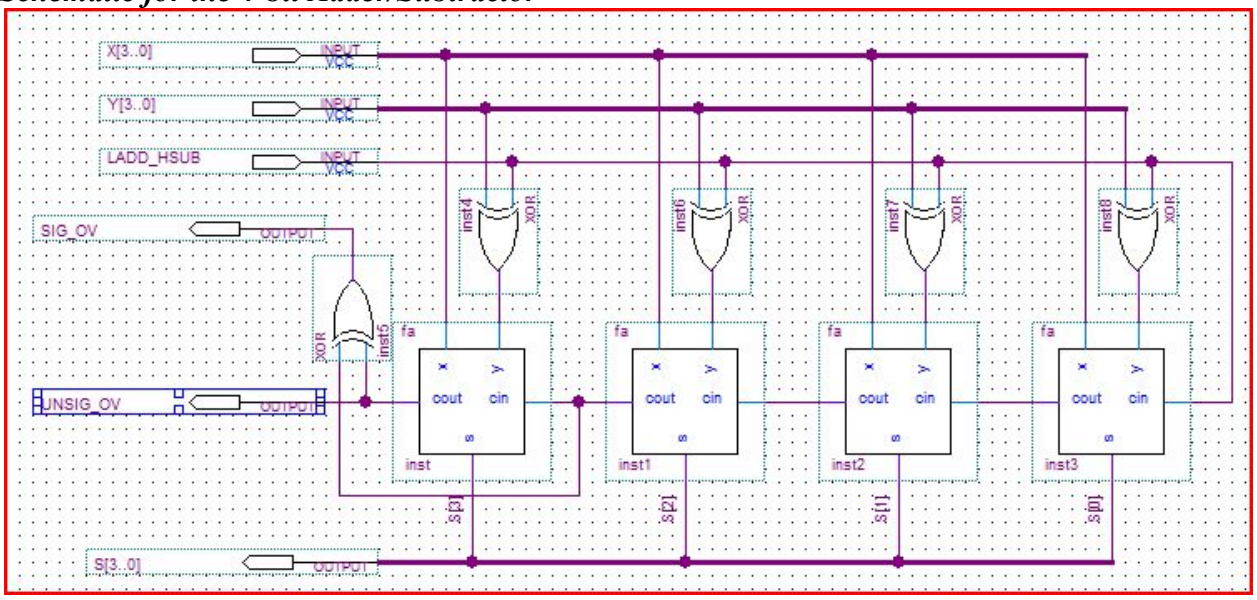
Exercise 1

Schematic for the 4-bit Adder/Subtractor

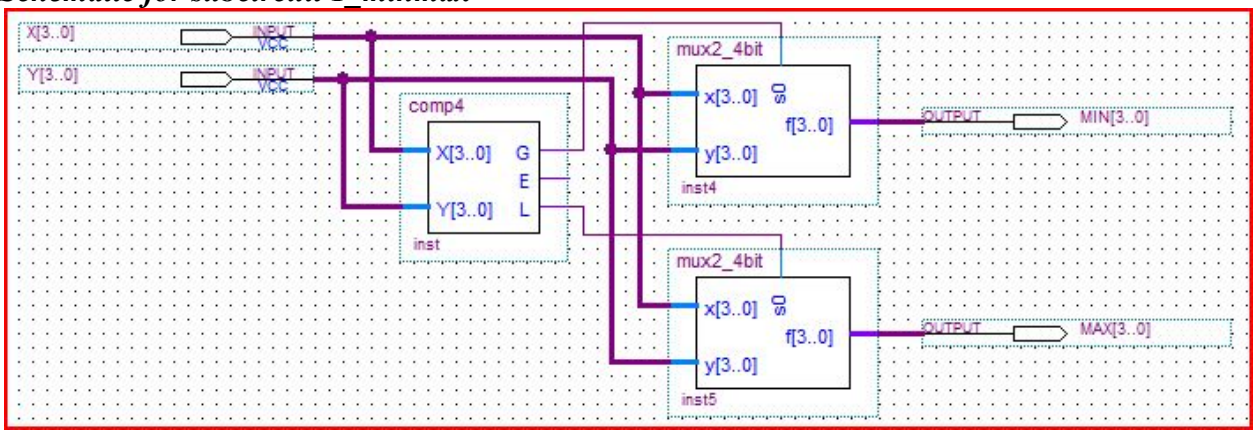


Functional Waveform for the 4-bit Adder/Subtractor

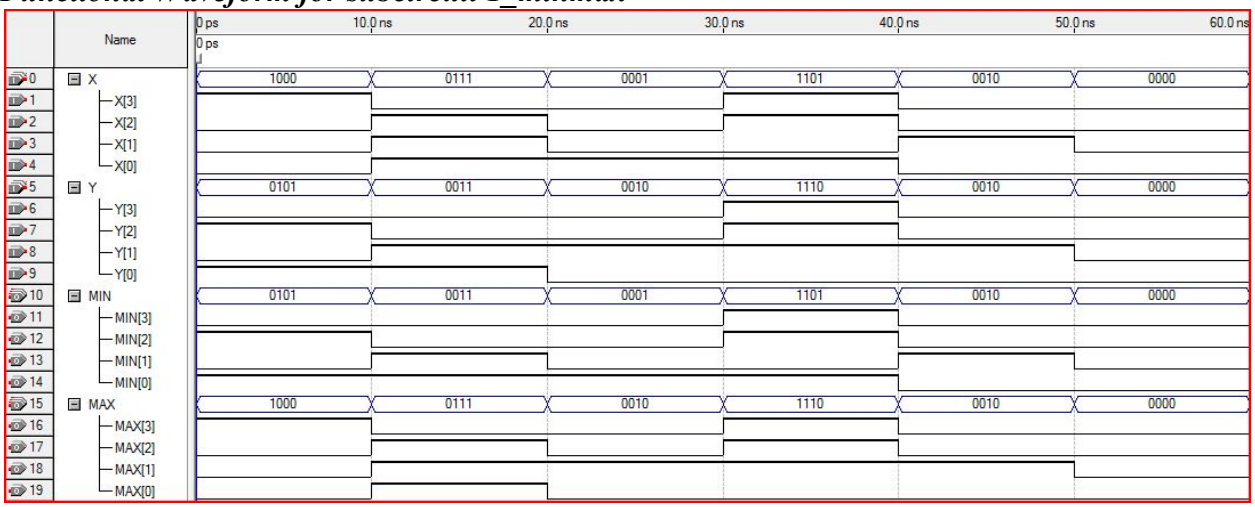
The waveform confirms that the Adder/Subtractor circuit is functional and can be used as a module in the ALU circuit.

Exercise 2

Schematic for subcircuit 1_minmax

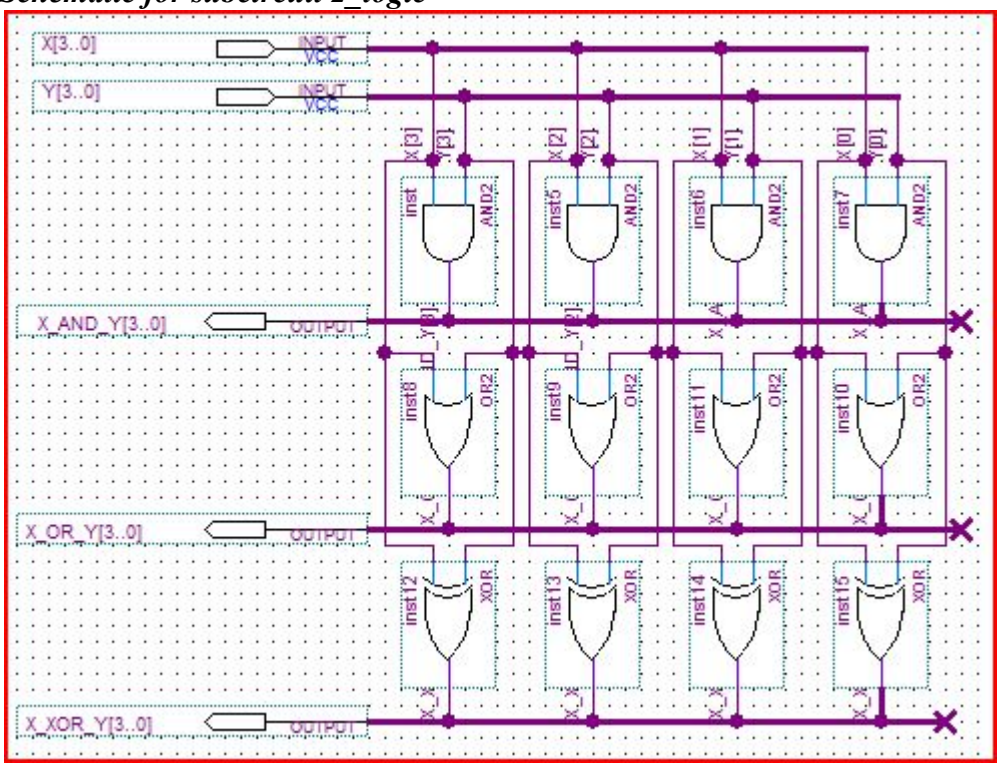


Functional Waveform for subcircuit 1_minmax

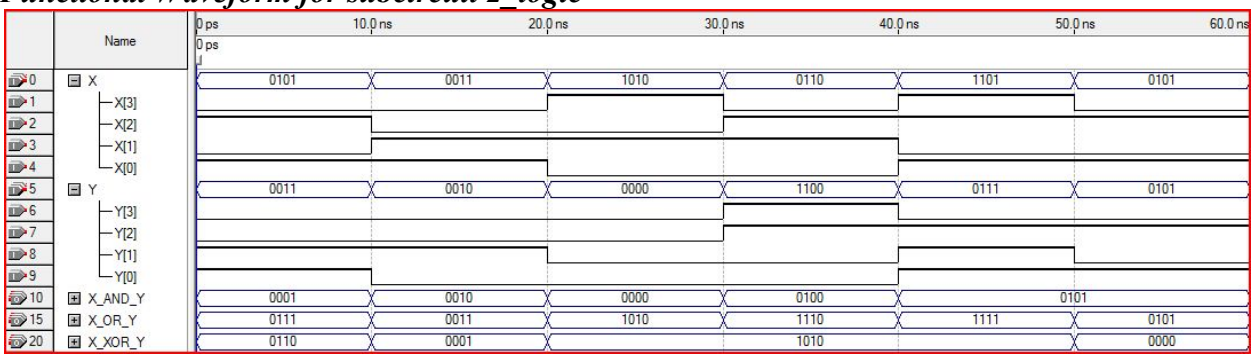


The waveform confirms that the minmax circuit is functional and can be used as a module in the ALU circuit.

Schematic for subcircuit 2_logic

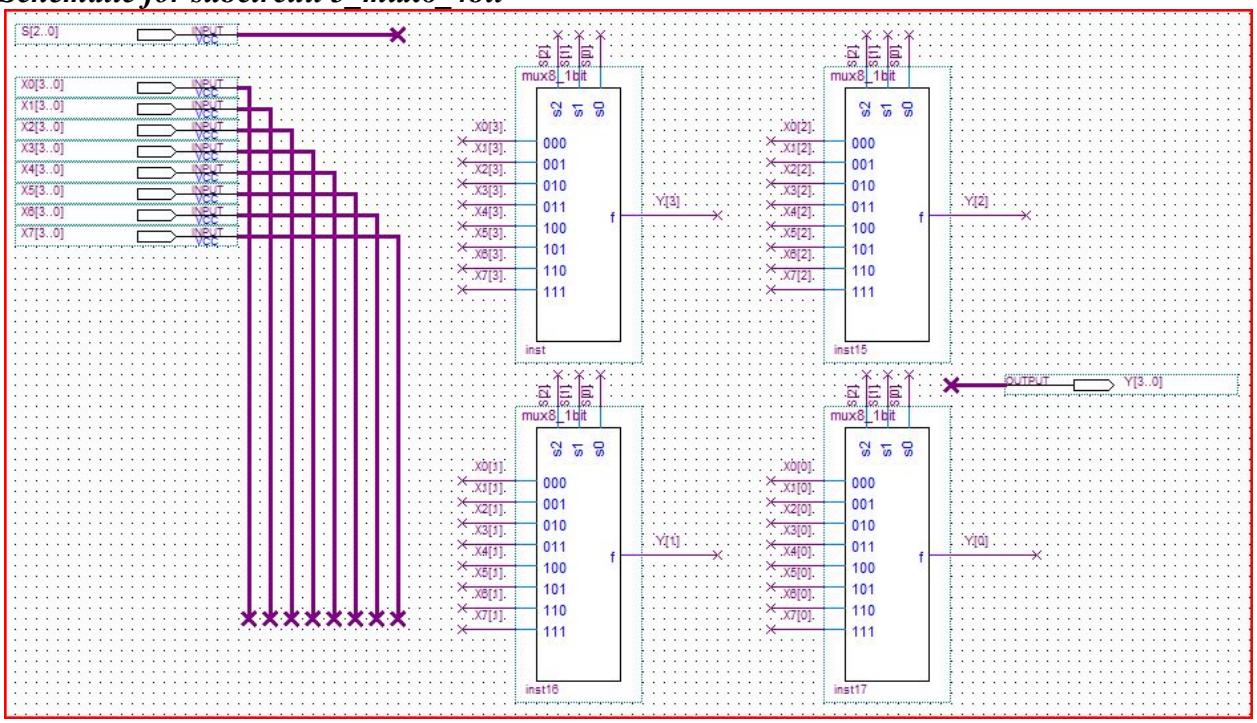


Functional Waveform for subcircuit 2_logic

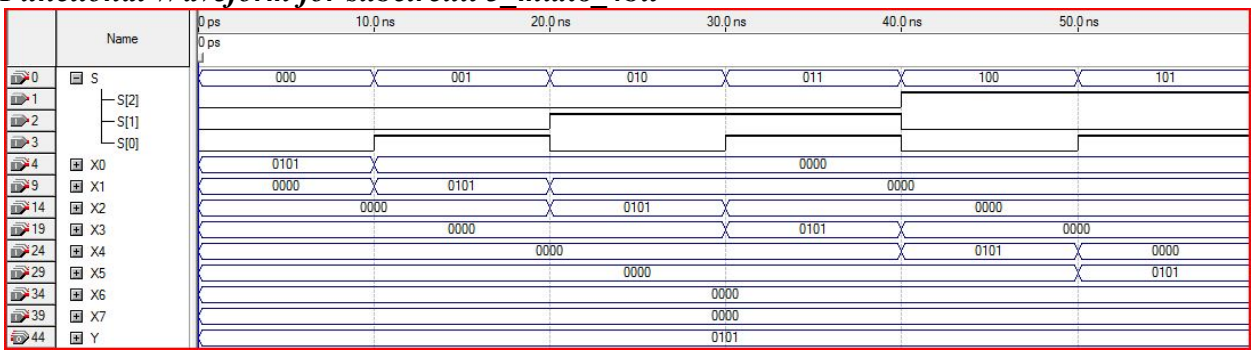


The waveform confirms that the logic circuit is functional and can be used as a module in the ALU circuit.

Schematic for subcircuit 3_mux8_4bit



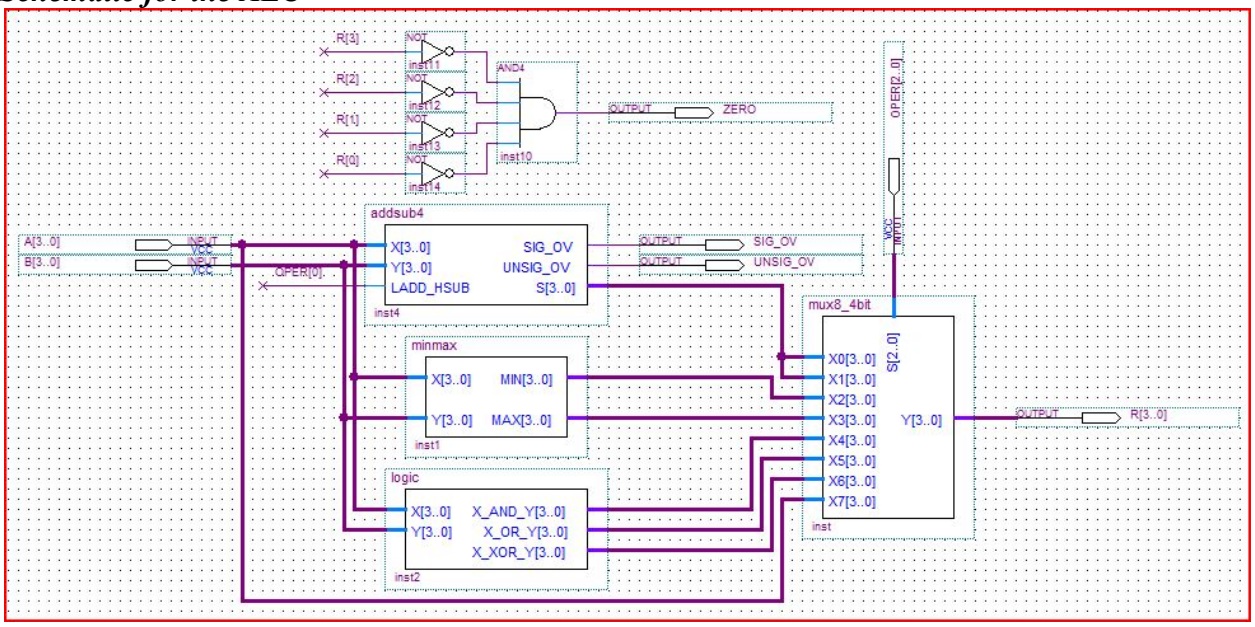
Functional Waveform for subcircuit 3_mux8_4bit



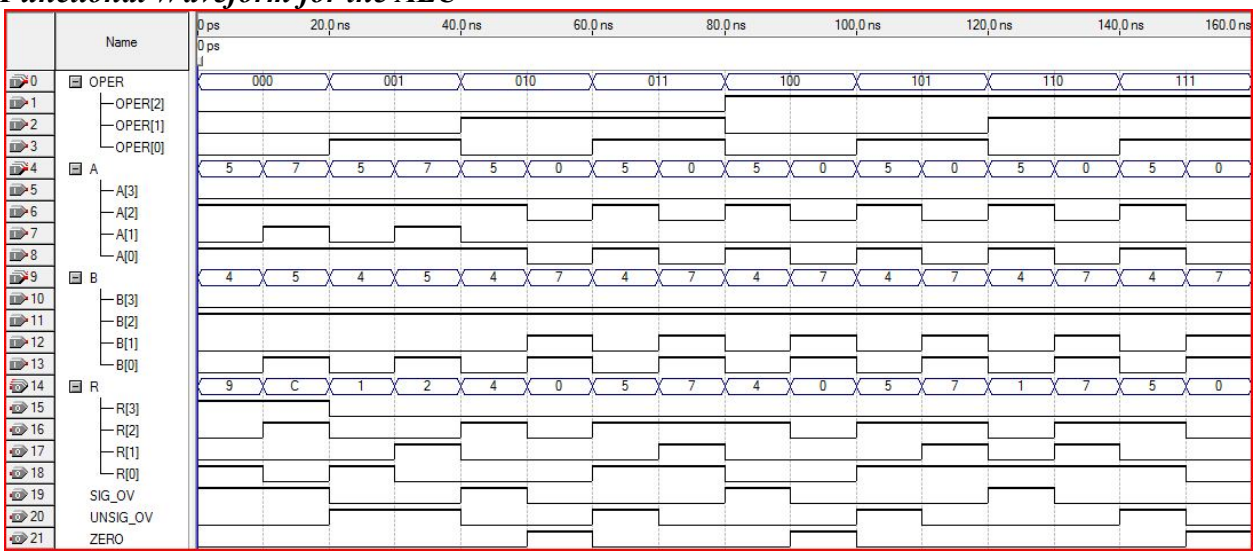
The waveform confirms that the 4bit 8-to-1 MUX is functional and can be used as a module in the ALU circuit.

Exercise 3

Schematic for the ALU

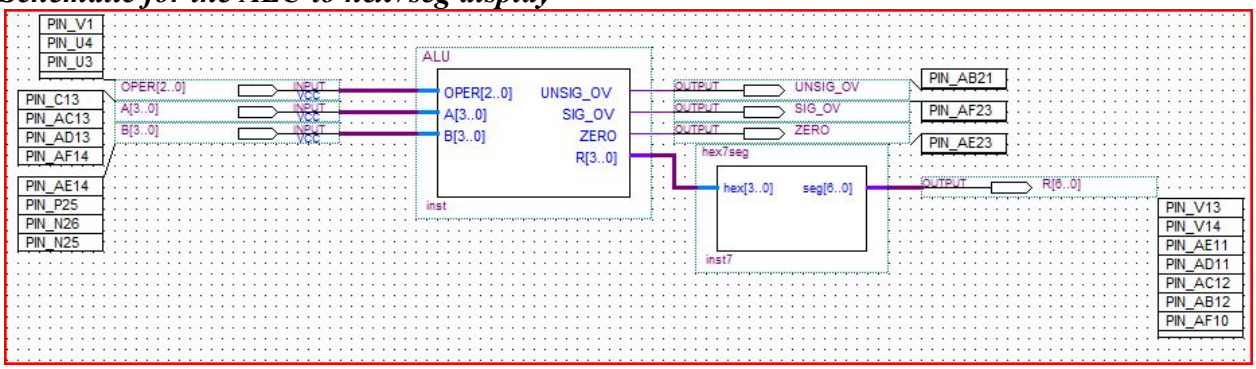


Functional Waveform for the ALU



The waveform shows that the ALU is functional and is ready to be uploaded to the DE2 board.

Schematic for the ALU to hex7seg display



The circuit was compiled and uploaded to the DE2 board and the correct results were shown on the HEX display and LEDs. Each module performs each task correctly and the ALU is functional.